

The Path of CMOS Image Sensor Technologies introduced to the Market

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Introduction

Image sensors are widely used in various kinds of applications. It is worthwhile to reflect on how image sensing technologies have evolved alongside the progress of these applications. Many of the foundational technologies in this field were originally proposed and refined by numerous researchers and institutions around the world, as highlighted by the significant contributions of early pioneers in the development of image sensor technology [1]. In this presentation, I will review the process of introducing these technologies to the market, acknowledging the essential groundwork laid by earlier researchers. This review, from my personal perspective as a member of Sony, focuses on integrating these foundational technologies into our products and bringing them to market.

The first application of CCD cameras was for airborne cameras, due to their vibration resistance and small form factor [2]. These advantages also enabled the development of professional and consumer camcorders. From the late 1990s, the major application for image sensors shifted to digital still cameras. Camera resolution increased every year, which means the pixel count of CCD image sensors also increased annually. Pixel shrinkage has been the main challenge in the development of CCD technology. Demands from digital still cameras accelerated CCD technologies and CCD technologies supported the growth of digital still cameras.

After the introduction of CMOS image sensors, the activities of searching for applications became more active.

First application for CMOS image sensor

The first generation of CMOS image sensor from Sony had 5 Tr pixel [3]. Due to its dot-sequential readout, fixed-pattern noise reduction and compact camera systems were realized. Consumer robots, cellular phone cameras, and other devices utilized these camera systems. On the other hand, this dot-sequential readout was applicable to VGA format because of its limited bandwidth.

Transition from CCD to CMOS image sensor I

When High-Definition TV became common, megapixel high-speed image sensors were needed. A critical issue was the heat generation in camcorders. To resolve this heat problem, HD camcorders began to adopt CMOS image sensors.

Another application change was occurring in DSLRs. The readout speed of CCDs was limited due to their large format. CMOS image sensors provided a well-balanced solution for both spatial and temporal resolutions.

During this transition, analog output column-parallel CDS readout CMOS image sensors were adopted. Camera developers could utilize their CCD-based camera systems.

Transition from CCD to CMOS image sensor II

High-speed HD video was the next challenge for CMOS image sensors. To achieve this significant increase in readout speed, a new column-parallel ADC readout was introduced. The dual in-line CDS architecture, which features both analog CDS and digital CDS in a serial fashion, enabled a readout speed more than 10 times faster while maintaining low noise simultaneously [4].

We aimed to realize the integration of still and video functions [5]. However, the spatial resolution was not sufficient for the still camera market.

Transition from CCD to CMOS image sensor III

1.75 μ m and 1.4 μ m pixels had been developed for the cellular phone market. Light pipe technology was also introduced to accommodate angled incident light [6]. Even with these technologies, further miniaturization of pixels and sensitivity improvements were necessary to replace CCD in the still camera market.

The solution to these challenges was the back-illuminated sensor technology. The introduction of this technology expanded from the video cameras to the still cameras and the cellular phone cameras. [7][8][9]

CMOS Image Sensor Approach I

Compared to digital still cameras and HD camcorders, cellular phone camera required different considerations. A compact and easy-to-implement camera module was provided for this largest camera market.

On-chip ADC became mandatory ahead of other applications. We applied column-parallel QV approach with fixed-pattern noise suppression circuit which achieved a noise level lower than that of CCDs [10].

CMOS Image Sensor Approach II

Gradually, column-parallel ADC readout and back-illuminated sensors were introduced to the cellular phone market. After the introduction of smartphones, the specifications and functionalities of cameras advanced. Consequently, the functionalities of CMOS image sensors also improved, and the circuit scale, including additional signal processing, became larger. A new challenge was how to harmonize both logic transistors and pixel performance. This motivated us to develop a stacked structure [11]. Independent wafer production for the pixel and circuit parts has significant advantages, as it allows us to optimize process conditions for both components.

In addition, the stacked structure offers further advantages. Utilizing wafer foundry services has enhanced our production capacity in response to the rapid market increase in smartphones. The stacked structure itself was also advanced from through-silicon vias (TSV) to Cu-Cu hybrid bonding. The number of stacking layers has increased from 2 layers to 3 layers [12].

Conclusion

The path of CMOS image sensor technologies to the market has been described. Technology development driven by market demands and the innovative creations of numerous pioneering researchers, has propelled the progress of both CMOS image sensor technologies and market.

The readout architecture of CMOS image sensors, starting from dot-sequential designs, has now evolved to pixel-parallel ADC. This signifies the evolution of functional parallelization.

In addition to this, device structure has also progressed from front-illuminated to back-illuminated, stacked and three-layer stacked sensors. This also represents process and production parallelization, in addition to functional parallelization. These evolutions in parallelization will lead to the further achievements

in image sensor technology.

References

- [1] A. Theuwissen, "There's More to the Picture Than Meets the Eye, and in the future it will only become more so," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 30-35.
- [2] <https://www.sony.com/en/SonyInfo/CorporateInfo/History/SonyHistory/2-11.html>
- [3] K. Yonemoto *et al.*, "A CMOS Image Sensor with a Simple Fixed-Pattern-Noise-Reduction Technology and a Hole Accumulation Diode," in *IEEE J. Solid-State Circuits*, vol.35, pp. 2038-2043, Dec. 2000.
- [4] Y. Nitta *et al.*, "High-speed digital double sampling with analog CDS on column parallel ADC architecture for low-noise active pixel sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 500-501.
- [5] S. Yoshihara *et al.*, "A 1/1.8-inch 6.4Mpixel 60 frames/s CMOS image sensor with seamless mode change," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, PP 492-493.
- [6] R. Fontaine *et al.*, "Trends in Consumer CMOS Image Sensor Manufacturing," in *Proc. Int. Image Sensor Workshop*, June 2009.
- [7] S. Iwabuchi *et al.*, "A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp.302-303.
- [8] <https://www.sony.jp/CorporateCruise/Press/200901/09-0115/>
- [9] H. Wakabayashi *et al.*, "A 1/2.3-inch 10.3 Mpixel 50frames/s back-illuminated CMOS image sensor," in *IEEE Int. Solid-State Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 410-411.
- [10] T. Haruta *et al.*, "A 1/3.2 Type 1.28M Pixel Low Power Consumption CMOS Image Sensor For Mobile Application," in *ITE Tech. Report*, Vol. 28, No.72, pp. 5-8, Nov. 2004.
- [11] S. Sukegawa *et al.*, "A 1/4-inch 8 Mpixel back-illuminated stacked CMOS image sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, PP. 484-485.
- [12] T. Haruta *et al.*, "A 1/2.3-inch 20 Mpixel 3-layer stacked CMOS image sensor with DRAM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 76-77.